EXHIBIT 1

Data Sheet

SYNOPSYS®

Astro

Advanced Physical Optimization, Placement and Routing Solution for System-on-Chip Designs

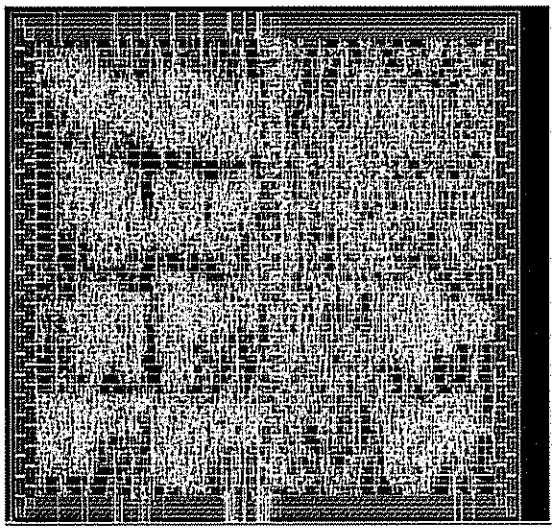
Overview

Numerous technology-dependent steps are required to complete a complex, ultra-deep-submicron integrated circuit (IC) design. Logic and interconnect delays must be analyzed and minimized. Physical effects such as signal crosstalk, power density,and supply voltage drop must be handled. Ideal clocks can no longer be assumed, and clock skew must be minimized. Physical effects are critical because changes to one may seriously impact the optimization of others. Moreover, a mistake seriously degrades circuit performance and manufacturability.

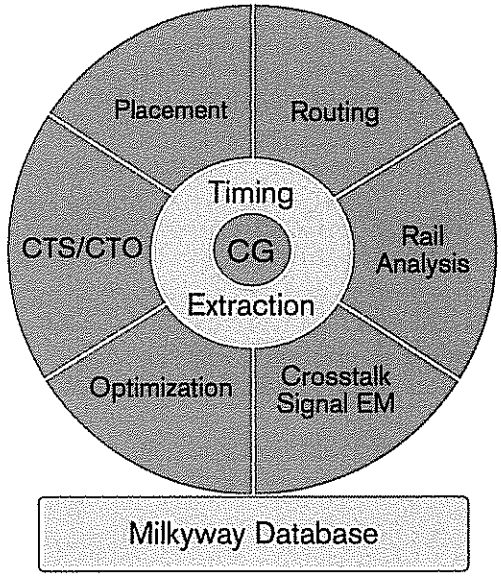
The Astro™ solution, Synopsys' advanced physical design system for optimization, placement and routing, uses a specialized architecture to concurrently account for physical effects while optimizing the resulting design. Even the largest IC designs are completed faster with Astro.

Astro Benefits

- Achieves Rapid Design Convergence. Astro's new Milkyway-DUO™ (Dynamic Unified Optimization) run-time representation provides a tight integration between physical optimization, layout (place and route), and analysis (timing, noise, rail) engines.
- Accounts for Ultra-Deep-Submicron Effects During Design Process. Astro's unique technology eliminatesiterations by concurrently accountingfor all physical effects throughout the design process.
- Increases Clock Speeds and Provides Faster Completion. Astro provides performance superior to Apollo-II™ and Saturn™, with an average of 10 percent faster clock speeds and up to 3X faster design completion.
- Improves Productivity and Ensures Lowest Clock Skew. Astro provides better control of placement change through incremental overlap removal and incremental placement. It also ensures the lowest possible clock skew with early timing and congestion impact prediction to boost productivity.
- Eliminates Migration Issues. Based on the Milkyway™ common database, Astro eliminates migration issues while providing direct "plug-and-play" into Synopsys' timing closure solution. Design data created with Synopsys' previous place and route generation tools is fully compatible with Astro.
- Handles Latest Manufacturing Process Rules. Astro handles the latest advanced process rules and thus improves design reliability. Antenna repair, via optimization, metal fill, and metal slotting are handled automatically. Effects such as conformal dielectrics, copper dishing, and shallow trench isolation are incorporated into the parasitic extraction engine.
- Shortens Design Cycles. New high-performance algorithms and distributed routing allow users to get designs out the door fast.



Integration of Astro's technology and Milkyway-DUO architecture offers simultaneous optimization of logic, interconnect delays, crosstalk, power, and clock issues.



Astro's new Milkyway-DUO architecture.

Astro's Technology Offers High Efficiency, Precise Correlation

Astro's concurrent technology is the advanced physical optimization technology used to achieve design closure. Astro predicts timing, signal integrity, power integrity, area, congestion, and routeability at every phase of the design, thus assuring design convergence as the physical solution evolves.

Astro technology integrates physical optimization, extraction, and analysis throughout place and route stages with high efficiency and precise correlation. This break-through technology resolves complex design issues, provides high-quality optimization results, and offers sign-off confidence in the final result. Astro delivers the optimal result faster and more efficiently.

Milkyway-DUO Offers Faster Run Times, Larger Design Capacity

The Milkyway database is the first step towards achieving timing closure. By eliminating data translation, the Milkyway-DUO architecture takes the integration of key design-closure tools to the next level. By using a compact run-time data structure on top of the Milkyway database, Astro ensures that all processes associated with specific optimization operations communicate synchronously with minimum database read/write. The Milkyway-DUO architecture uses dynamically allocated, shared memory to reduce run times and increase design capacity.

Advanced Timing Engine Eliminates Iterations

A new, advanced timing engine is at the heart of the Astro architecture. Tight integration of this fully incremental timing engine with the optimization, placement and routing engines eliminates iterations, thereby ensuring a consistent view of timing and reducing design turnaround time Astro's timing engine offers designers the following benefits:

- Catches timing-constraint errors early through constraint checking
- Checks static timing analysis correlation with Star-Hspice™ and PrimeTime™ throughout the place and route flow
- Eliminates translation inconsistencies by directly accepting SDC and .lib files
- Offers rapid design convergence with highly accurate parasitic extraction
- Eliminates timing discrepancies by using an accurate delay calculation engine whose results are within five percent of Star-Hspice
- Handles delay crosstalk effects based on accurate parasitics
- Ensures fast updates during physical optimizations with incremental timing analysis
- Provides a dramatic increase in speed and reduces memory requirements

New Placement Engine is Important Component of Astro

A new placement engine, an important part of the Astro design-closure solution, delivers the high quality results that designers require This engine resolves the majority of timing issues by optimizing placement for minimal wire length and delay. Moreover, advanced placement is used for signal-integrity prevention and analysis. The new placement engine provides:

- Shorter wire length and less congestion to reduce the time and effort required for routing
- Concurrent optimization of signal integrity, physical optimization, and clock tree results

Users can expect up to 25 percent shorter wire length, significantly less memory usage, greatly reduced congestion, and a 25 percent faster run time for the detailed placement engine compared with Apollo-II. The incremental placement capability handles large-scale engineering-change-order (ECO) placement changes more efficiently, minimizing their impact on layout and timing

Clock Tree Synthesis–Most Critical Nets in IC Design

Clock nets are the most critical nets in a design. In today's high-speed SoC designs, clocking schemes are complex and clock-skew requirements are exceedingly stringent As design sizes increase and clock speeds exceed 1 GHz, clock trees require extreme care to prevent disturbance caused by congestion and timing optimization. The benefits of Astro's clock-tree synthesis engine include:

- Efficient clock tuning through local skew analysis and optimization
- Streamlining ECOs through incremental overlap removal, incremental placement and incremental clock tree synthesis and optimization

Astro-Xtalk, Astro-Rail: Options for Power Integrity and Signal Integrity

Astro-Xtalk™, the signal-integrity option to Astro, is the most comprehensive solution to signal-integrity issues available for ultra-deep submicron designs. Astro-Rail™, the power-integrity option to Astro, provides the most comprehensive and complete solution for power consumption, IR-drop, and electromigration issues in UDSM designs. For additional information on these options, please see their respective datasheets.

Ideally Suited to CAD Environments

Astro is designed for seamless integration into existing computer-aided-design (CAD) flows and environments.

Utilizing Synopsys' Milkyway common database, Astro works seamlessly with JupiterXT™ for hierarchical design planning, the Astro-Xtalk option for signal integrity analysis/prevention/correction, the Astro-Rail option for power-driven layout and rail analysis, Design VERIFYer™ for formal equivalence checks, Star-RCXT™ for 3-D extraction, Hercules™ for physical verification and DRC repair, Enterprise™ for full-custom layout editing, and Columbia™ for top-level chip assembly

Easy Transition from Apollo-II to Astro

Both Astro and Apollo-II are based on Synopsys' Milkyway common database, thereby ensuring complete database compatibility. Designers can seamlessly switch existing designs, either in process or completed, from Apollo-II to Astro to enjoy the overall superior performance of Astro.

Astro solves today's and tomorrow's design-closure challenges as a result of Synopsys' investment in advanced research and development, outstanding development team, and field experience from previous generations of solutions. The result is the Astro advanced optimization, placement and routing solution to achieve rapid design closure for the most demanding designs in leading-edge technologies.

For more information about Synopsys products, support services or training, visit us on the web at www.synopsys.com, contact your local sales representative or call 650.584.5000.

SYNOPSYS®

EXHIBIT 2

Products

> JupiterIO
> Hard Macro Placement in Complex SoC Design
> Galaxy Power Brochure
> Multi Voltage Technology Backgrounder
> Power Management White Paper

Press Releases

> Synopsys Expands University Program by Donating Technology
> Synopsys Unveils Galaxy IC Compiler
> ARM and Synopsys Announce Industry-First and Recommended Flow for ARM11 Family
> Synopsys Announces Support for SUSE Linux
> Chipidea Licenses Synopsys' Galaxy Design and Discovery Verification Platforms
> Toshiba Achieves 40 Percent Power Reduction in Latest MeP SoC with Synopsys Galaxy Design Platform
> Sasken Develops Reference Flow Based on Synopsys' Galaxy Design Platform

Customer Education

> JupiterXT Customer Training

Related Links

> Galaxy and Discovery Platforms
> Platform Releases
> Office Locations
> SolvNet
> Search for IP
> SVP Cafe
> SNUG

Galaxy Design Planning

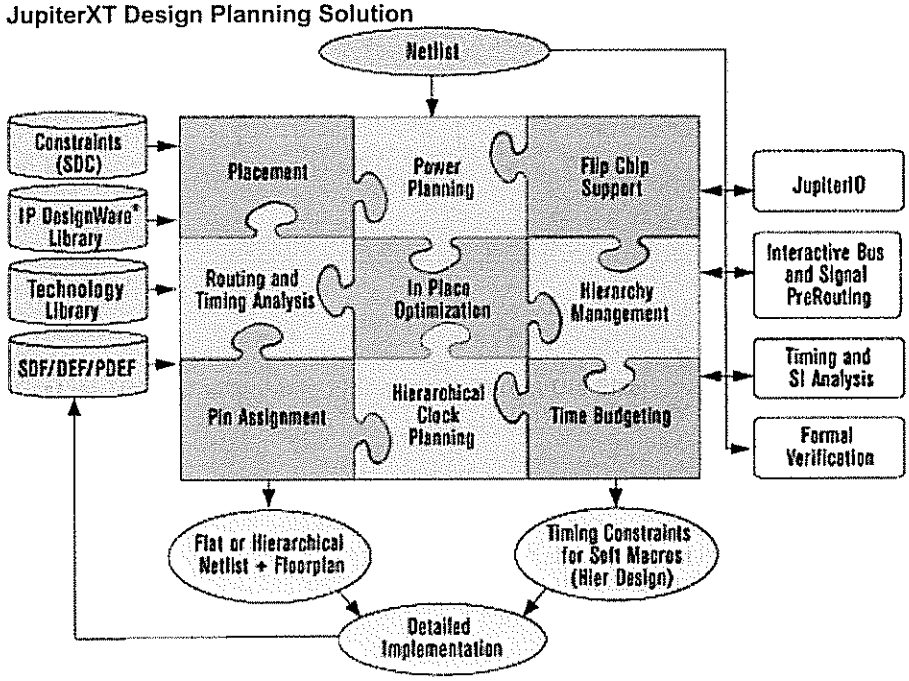
JupiterXT

Fastest Time to a Routable Floorplan in Target Die Size

Overview

Synopsys' JupiterXT™ design planning solution enables fast feasibility analysis for a preview of implementation results, and provides detailed floorplanning capabilities for flat or hierarchical physical design implementation styles. Project leaders and physical designers of ASIC or COT designs benefit from the accurate prediction and production-proven convergence JupiterXT provides.

JupiterXT Design Planning Solution



Feasibility analysis is supported for incomplete netlists in the form of black boxes or early gate level netlists. The powerful placement algorithms incorporate designers' knowledge of black box content and produce floorplan results using autoshaping with full rectilinear support. For early gate level netlists, the placement algorithms apply a virtual flat approach that places hard macros and standard cells simultaneously.

As more detailed design content is added to netlists as a result of module synthesis, the feasibility results are reused to guide detailed floorplanning. The core placement, routing analysis, and timing analysis engines are common to Synopsys' proven detailed implementation tools, Physical Compiler® and Astro™, ensuring the fastest convergence to routable, timing correct floorplans. Design and library data is read and written from Synopsys' Milkyway™ database enabling fast and efficient transfers into and from the design planning tool.

For flat and hierarchical implementation styles, JupiterXT provides macro placement, power network synthesis and analysis, routing analysis, in-place optimization, and timing analysis capabilities. Additionally, for hierarchical implementation styles, JupiterXT provides hierarchy management, pin assignment, and time budgeting

capabilities

Key Benefits

- Fast and accurate feasibility studies via full black box support - from placement through autoshaping, timing and time budgeting
- Feasibility of early gate-level netlists via fast, virtual flat placement
- Predictability to Physical Compiler and Astro implementation results due to common placement, routing, and timing engines for feasibility and detailed floorplanning
- Capacity and runtime to address your largest designs
- Increased productivity with technology advancements, including automatic hardmacro and standard cell placement, along with power network synthesis
- No wasted feasibility work because core engines shared with production-proven Physical Compiler and Astro tools ensure convergence and correlation of results
- Support of your proprietary design flows with multiple physical design methodologies: flat, hierarchical, top-down, virtual-flat, abutted, and channeled

Design Challenges

As new process nodes are introduced, larger and larger designs are possible. With increasing design sizes, more complex SoC systems are being designed. To handle the large number of gates in a design, designers are using more hard macros. Clock speeds on designs are on the rise-some operating in the GHz range. Leakage currents of devices at smaller process nodes are also increasing. These are just some of the technical factors contributing to the increased complexity of today's SoC design starts. Additionally, market pressures are unrelenting and the time available for design teams to get from RTL to GDSII is shrinking. Design teams are faced with implementing larger, more complex designs, while dealing with placement, routing, timing, and power closure, in shorter periods of time. The challenges addressed by JupiterXT design planning are:

- The need to assess the feasibility of larger, faster, more power hungry designs
- The need to finalize design floorplans in shorter amounts of time in the smallest possible dies

Solution

The Synopsys solution for today's SoC design challenges is the Galaxy Design Platform. The Design Planning solution within the platform is JupiterXT. The JupiterXT Design Planning solution provides the capacity to handle the largest designs.

Supports Fast Feasibility Analysis

Full black box support with automatic shaping and rectilinear awareness enables fast feasibility analysis of die size, top-level routing, and top-level timing characteristics. For early gate level netlists, the virtual flat placement capabilities produce results quickly. Assess the potential to meet critical timing requirements early using in-place optimization.

Power Network Analysis for Fast and Easy Power Network Refinement

The breakthrough power network synthesis and analysis functions, applied during the feasibility phase of design planning, lead to power networks that meet or exceed voltage drop and electro migration requirements. These functions are native to JupiterXT and tightly correlated with Astro-Rail, eliminating the need to perform ASCII or binary design data transfers to other tools to perform voltage drop and electromigration analysis. Therefore, during detailed floorplanning, the power network synthesis and analysis functions enable fast and easy checking and refinement of the power network as netlist updates come in.

Macro Placement Makes Floorplanning Easy

Using the patented conjugate gradient placement algorithm from Physical Compiler in JupiterXT to automatically place both hard macros and standard cells at the same time essentially eliminates intensive manual iteration. It makes detailed floorplanning simply easier and converges to quality results more quickly.

Correlation with Physical Compiler and Astro
Tight correlation of feasibility studies and detailed floorplanning to detailed implementation results come from using the same core engines as the detailed implementation tools. JupiterXT's core placement, routing analysis, and timing analysis engines are from Synopsys' production-proven Physical Compiler and Astro tools.

Supports Multiple Physical Implementation Design Styles
The JupiterXT Design Planning solution supports multiple physical implementation design styles. For flat styles, the placement, power network synthesis and analysis, routing analysis, timing analysis, and in place optimization functions are applied to quickly converge on initial placements to pass forward to detailed optimization tools For hierarchical styles, JupiterXT supports hierarchy management tools, virtual flat or top-down flows, channeled or abutted floorplans, and time budgeting. The flexibility provided enables design teams to apply their proprietary physical design implementation styles the way they prefer.

Support for Flip Chip Designs
JupiterIO is a concurrent die/package IO (input/output) planning solution that provides a unified view of both die and package data within a single tool for the purpose of coordinated IO planning and package feasibility for complex flip chip designs. JupiterIO includes IO and bump placement, redistribution layer (RDL) routing, and package route planning capabilities.

Related Products

- Astro
- Design Compiler
- Encore
- Formality
- JupiterIO
- Milkyway
- IC Compiler
- Physical Compiler
- PrimeRail
- PrimeTime

EXHIBIT 3

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December 13, 2005

VIA FACSIMILE (650-813-4848) AND U.S. MAIL

Michael Edelman, Esq.
Dechert LLP
975 Page Mill Road
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Re: Synopsys v. Magma, et al

Dear Mr. Edelman:

This is in response to your letter of December 9, which was delivered to us at the end of the day last Friday, along with 134 data disks. Some of those disks (Nos. 11, 107-9, 111, 116 and 132) are corrupted and cannot be read.

In addition to providing readable replacements, please provide an index, so that we can understand what you have included on these disks. Moreover, please specify, by bates range, which documents are responsive to which document requests.

We note your concerns regarding overbreadth and burden. We have similar concerns about the discovery requests that you propounded. We are happy to host a meeting to discuss all these issues. Would tomorrow afternoon work for you?

In your final paragraph, you state that "these responsive documents are available for use in this litigation and Synopsys will proceed accordingly." If by that you mean to say that you are relieved of the restraints of the protective order in the California case, we do not agree. If you wish to pursue that subject, please contact counsel of record in that matter. On a related point, and further to our recent discussion about document production in which you raised a concern about access to Magma's source code, we will consent to your having access to the Magma code

produced in the California case, on the condition that you provide us with a copy of the Synopsys source code on a date certain within the next two weeks. If you believe that would be impractical, we would want at a minimum to have the source code, including a fully functional copy, for IC Compiler, Design Compiler, Physical Compiler, Galaxy Design Platform, Milkyway database, Milkyway-DUO, DFT Compiler, and Astro, including all supporting code and routines necessary to run these applications.

Finally, we have not heard back from you concerning the proposed protective order we sent on December 1. Please let us have any comments in the next two days, so that we can be prepared if necessary to address issues of disagreement when we are before the Court next Monday.

Very truly yours,

FOR

James Pooley

JP:lel